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10/765,993	01/29/2004	Hidenori Nanki	56937-106	2852

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Washington, DC 20005-3096

EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,993	NANKI ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 11-22, 29-40* is/are rejected.

7)☒ Claim(s) *5-10 and 23-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 are pending and have been examined.

2. Claims 1-4, 11-22 and 29-40 are rejected.

3. Claims 5-10 and 23-28 are objected to.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

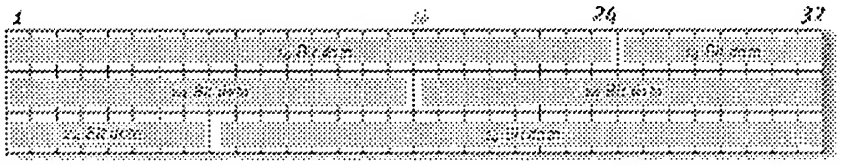
5. Claims 1-4, 11-22 and 29-40 rejected under 35 U.S.C. 102(b) as being anticipated by TerraTec's "SoundSystem DMX 6fire 34/69" (hereinafter DMX).

For claims 1 and 19:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- converting M-bit format data, which is a basic data unit for data processing, to N-bit format data, which is a basic data unit for data transmission; and
- transmitting the converted N-bit format data to a data processing device (page 31; DMX discloses M-bit format data, that is a basic data unit for data processing, is 24-bit audio data [paragraph 3]. "Audio data streams are transferred to the computer's main memory

via the PCI bus. The PCI bus features 32 'lines' (32-bit) [paragraph 2]." "The '24-bit packed' process solves this problem in the following manner: the computer CPU (your Pentium for example) divides the 24-bit data into multiples of 32 (middle diagram) [paragraph 3]." In other words DMX discloses audio data of 24-bit data is converted to 32-bit data by creating packets consisting of multiple 24-bit words of data in the format shown below:



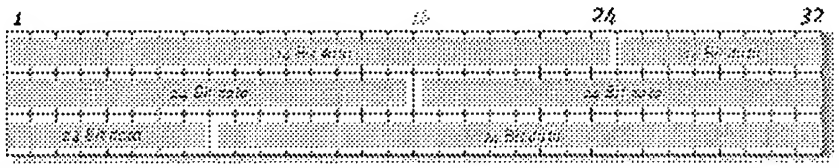
A first 32-bit data packet is constructed of an entire 24-bit audio data word followed by the first 8-bits of a second audio data word. A second 32-bit data packet is constructed of the remaining 16-bits of the second 24-bit audio data word and the first 16-bits of a third audio data word. Finally a third 32-bit data packed is constructed of the remaining 8-bits of the third 24-bit audio data word and an entire fourth 24-bit audio data word. As such M-bit format data [24-bit audio data] is converted to N-bit format [32-bit PCI format data] for transmission to a data processing device.).

For claims 2 and 20:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- transmitting N-bit format data, which is a basic data unit for data transmission, from a data processing device; and
- converting the transmitted N-bit format data to M-bit format data, which is a basic data unit for data processing (page 31; DMX discloses M-bit format data, that is a basic data

unit for data processing, is 24-bit audio data [paragraph 3]. "Audio data streams are transferred to the computer's main memory via the PCI bus. The PCI bus features 32 'lines' (32-bit) [paragraph 2]." "The '24-bit packed' process solves this problem in the following manner: the computer CPU (your Pentium for example) divides the 24-bit data into multiples of 32 (middle diagram) [paragraph 3]." In other words DMX discloses audio data of 24-bit data is converted to 32-bit data by creating packets consisting of multiple 24-bit words of data in the format shown below:



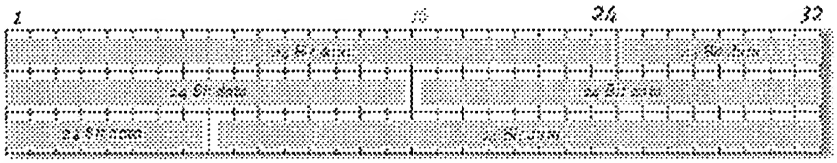
A first 32-bit data packet is constructed of an entire 24-bit audio data word followed by the first 8-bits of a second audio data word. A second 32-bit data packet is constructed of the remaining 16-bits of the second 24-bit audio data word and the first 16-bits of a third audio data word. Finally a third 32-bit data packed is constructed of the remaining 8-bits of the third 24-bit audio data word and an entire fourth 24-bit audio data word. As such M-bit format data [24-bit audio data] is converted to N-bit format [32-bit PCI format data] for transmission to a data processing device.).

For claims 3 and 21:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- converting N-bit format data, which is a basic data unit for data transmission, to M-bit format data, which is a basic data unit for data processing; and

- writing the converted M-bit format data in a buffer memory (page 31; DMX discloses M-bit format data, that is a basic data unit for data processing, is 24-bit audio data [paragraph 3]. "Audio data streams are transferred to the computer's main memory via the PCI bus. The PCI bus features 32 'lines' (32-bit) [paragraph 2]." "The '24-bit packed' process solves this problem in the following manner: the computer CPU (your Pentium for example) divides the 24-bit data into multiples of 32 (middle diagram) [paragraph 3]." In other words DMX discloses audio data of 24-bit data is converted to 32-bit data by creating packets consisting of multiple 24-bit words of data in the format shown below:

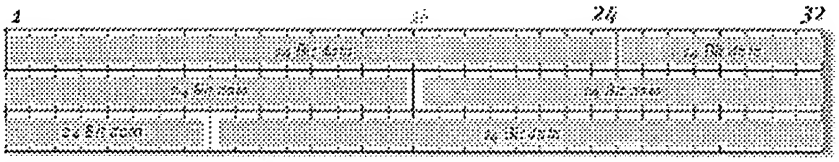


A first 32-bit data packet is constructed of an entire 24-bit audio data word followed by the first 8-bits of a second audio data word. A second 32-bit data packet is constructed of the remaining 16-bits of the second 24-bit audio data word and the first 16-bits of a third audio data word. Finally a third 32-bit data packed is constructed of the remaining 8-bits of the third 24-bit audio data word and an entire fourth 24-bit audio data word. As such M-bit format data [24-bit audio data] is converted to N-bit format [32-bit PCI format data] for transmission to a data processing device.).

For claims 4 and 22:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- reading M-bit format data, which is a basic data unit for data processing, from a buffer memory; and
- converting the M-bit format data thus read to N-bit format data, which is a basic data unit for data transmission (page 31; DMX discloses M-bit format data, that is a basic data unit for data processing, is 24-bit audio data [paragraph 3]. "Audio data streams are transferred to the computer's main memory via the PCI bus. The PCI bus features 32 'lines' (32-bit) [paragraph 2]." "The '24-bit packed' process solves this problem in the following manner: the computer CPU (your Pentium for example) divides the 24-bit data into multiples of 32 (middle diagram) [paragraph 3]." In other words DMX discloses audio data of 24-bit data is converted to 32-bit data by creating packets consisting of multiple 24-bit words of data in the format shown below:



A first 32-bit data packet is constructed of an entire 24-bit audio data word followed by the first 8-bits of a second audio data word. A second 32-bit data packet is constructed of the remaining 16-bits of the second 24-bit audio data word and the first 16-bits of a third audio data word. Finally a third 32-bit data packed is constructed of the remaining 8-bits of the third 24-bit audio data word and an entire fourth 24-bit audio data word. As such M-bit format data [24-bit audio data] is converted to N-bit format [32-bit PCI format data] for transmission to a data processing device.).

For claims 11, 29, 37 and 39:

A data transmission method, which processes data through an N-bit bus, comprising a multi-format conversion step of:

- dividing M-bit format data into packets of s-bits that correspond to the greatest common measure of M and N; and
- converting q-number of data having an M-bit format constituted by s bits × p packets to p-number of data having an N-bit format constituted by s bits × q packets, by using r-number of packets corresponding to the least common multiple of M ÷ s =p and N ÷ s=q as one unit (page 31; DMX discloses M-bit format data, that is a basic data unit for data processing, is 24-bit audio data [paragraph 3]. "Audio data streams are transferred to the computer's main memory via the PCI bus. The PCI bus features 32 'lines' (32-bit) [paragraph 2]." "The '24-bit packed' process solves this problem in the following manner: the computer CPU (your Pentium for example) divides the 24-bit data into multiples of 32 (middle diagram) [paragraph 3]." In other words DMX discloses audio data of 24-bit data is converted to 32-bit data by creating packets consisting of multiple 24-bit words of data. A first 32-bit data packet is constructed of an entire 24-bit audio data word followed by the first 8-bits of a second audio data word. A second 32-bit data packet is constructed of the remaining 16-bits of the second 24-bit audio data word and the first 16-bits of a third audio data word. Finally a third 32-bit data packed is constructed of the remaining 8-bits of the third 24-bit audio data word and an entire fourth 24-bit audio data word. As such M-bit format data [24-bit audio data] is converted to N-bit format [32-bit PCI format data] for transmission to a data processing device.).

For claims 12, 30, 38 and 40:

A data transmission method, which processes data through an N-bit bus, comprising a multi-format conversion step of:

- dividing N-bit format data into packets of s-bits that correspond to the greatest common measure of N and M; and
- converting p-number of data having an N-bit format constituted by s bits × q packets to q-number of data having an M-bit format constituted by s bits × p packets, by using r-number of packets corresponding to the least common multiple of M ÷ s=p and N ÷ s=q as one unit (page 31; DMX discloses M-bit format data, that is a basic data unit for data processing, is 24-bit audio data [paragraph 3]. "Audio data streams are transferred to the computer's main memory via the PCI bus. The PCI bus features 32 'lines' (32-bit) [paragraph 2]." "The '24-bit packed' process solves this problem in the following manner: the computer CPU (your Pentium for example) divides the 24-bit data into multiples of 32 (middle diagram) [paragraph 3]." In other words DMX discloses audio data of 24-bit data is converted to 32-bit data by creating packets consisting of multiple 24-bit words of data. A first 32-bit data packet is constructed of an entire 24-bit audio data word followed by the first 8-bits of a second audio data word. A second 32-bit data packet is constructed of the remaining 16-bits of the second 24-bit audio data word and the first 16-bits of a third audio data word. Finally a third 32-bit data packed is constructed of the remaining 8-bits of the third 24-bit audio data word and an entire fourth 24-bit audio data word. As such M-bit format data [24-bit audio data] is converted to N-bit format [32-bit PCI format data] for transmission to a data processing device.).

For claims 13-18 and 31-36:

The data transmission method according to claims 1-4, 11-12, 19-22 and 29-30, wherein the N-bit bus is a 32-bit bus, the N-bit format data is 32-bit format data and the M-bit format data 24-bit format data (*please see the rejections above regarding DMX and conversion between M-bit audio data and N-bit data for transmission over a PCI bus*).

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-4, 11-12, 19-22, 29-30 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (US5768546).

Claims 1-18 are substantially equivalent to claims 19-36 in that claims 1-18 represent the method of operating the apparatus of claims 19-36. As such, claims 19-36 will be rejected on the same basis as those presented for claims 1-18.

For claims 1 and 19:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- converting M-bit format data, which is a basic data unit for data processing (Although not explicitly disclosed in Kwon, it is obvious to one of ordinary skill in the art that at least

one processor circuit is connect to the system bus [Fig. 2, item 1]. The system bus is known in the art to be the communication bus to which processor and memory devices are connected because of the increased performance associated with a system bus, as opposed to a peripheral bus. The system bus supports 32-bit words from processor devices attached thereto. Therefore it is obvious that 32-bits is the "basic data unit for data processing" of devices attached to the system bus. As such Kwon successfully teaches M-bit format data which is a basic data unit for data processing.), to N-bit format data (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36); and

- transmitting the converted N-bit format data, which is a basic data unit for data transmission (Kwon teaches the second system bus [Fig. 2, 12] only supports transmission of data in 16-bit data words [col. 3, ll. 59-63]. Therefore the 16-bit data words of the second system bus represent a "basic data unit for data transmission" across the second system bus thus meeting the claimed limitation.), to a data processing device (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36).

For claims 2 and 20:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- transmitting N-bit format data which is a basic data unit for data transmission (Kwon teaches the second system bus [Fig. 2, 12] only supports transmission of data in 16-bit data words [col. 3, ll. 59-63]. Therefore the 16-bit data words of the second system bus represent a "basic data unit for data transmission" across the second system bus thus

meeting the claimed limitation.), from a data processing device (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36); and

- converting the transmitted N-bit format data to M-bit format data, which is a basic data unit for data processing (Although not explicitly disclosed in Kwon, it is obvious to one of ordinary skill in the art that at least one processor circuit is connect to the system bus [Fig. 2, item 1]. The system bus is known in the art to be the communication bus to which processor and memory devices are connected because of the increased performance associated with a system bus, as opposed to a peripheral bus. The system bus supports 32-bit words from processor devices attached thereto. Therefore it is obvious that 32-bits is the "basic data unit for data processing" of devices attached to the system bus. As such Kwon successfully teaches M-bit format data which is a basic data unit for data processing.) (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36).

For claims 3 and 21:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- converting N-bit format data, which is a basic data unit for data transmission (Kwon teaches the second system bus [Fig. 2, 12] only supports transmission of data in 16-bit data words [col. 3, ll. 59-63]. Therefore the 16-bit data words of the second system bus represent a "basic data unit for data transmission" across the second system bus thus meeting the claimed limitation.), to M-bit format data, which is a basic data unit for data processing (Although not explicitly disclosed in Kwon, it is obvious to one of ordinary skill in the art that at least one processor circuit is connect to the system bus [Fig. 2, item

1]. The system bus is known in the art to be the communication bus to which processor and memory devices are connected because of the increased performance associated with a system bus, as opposed to a peripheral bus. The system bus supports 32-bit words from processor devices attached thereto. Therefore it is obvious that 32-bits is the "basic data unit for data processing" of devices attached to the system bus. As such Kwon successfully teaches M-bit format data which is a basic data unit for data processing.) (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36); and

- writing the converted M-bit format data in a buffer memory (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36).

For claims 4 and 22:

A data transmission method, which processes data through an N-bit bus, comprising the steps of:

- reading M-bit format data, which is a basic data unit for data processing (Although not explicitly disclosed in Kwon, it is obvious to one of ordinary skill in the art that at least one processor circuit is connect to the system bus [Fig. 2, item 1]. The system bus is known in the art to be the communication bus to which processor and memory devices are connected because of the increased performance associated with a system bus, as opposed to a peripheral bus. The system bus supports 32-bit words from processor devices attached thereto. Therefore it is obvious that 32-bits is the "basic data unit for data processing" of devices attached to the system bus. As such Kwon successfully teaches M-bit format data which is a basic data unit for data processing.), from a buffer memory (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36); and

- converting the M-bit format data thus read to N-bit format data, which is a basic data unit for data transmission (Kwon teaches the second system bus [Fig. 2, 12] only supports transmission of data in 16-bit data words [col. 3, ll. 59-63]. Therefore the 16-bit data words of the second system bus represent a "basic data unit for data transmission" across the second system bus thus meeting the claimed limitation.) (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36).

For claims 11, 29, 37 and 39:

A data transmission method, which processes data through an N-bit bus, comprising a multi-format conversion step of:

- dividing M-bit (16) format data into packets of s-bits (8) that correspond to the greatest common measure of M (16) and N (32) (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36); and
- converting q-number (4) of data having an M-bit format constituted by s (8) bits × p (2) packets to p-number (2) of data having an N-bit format constituted by s bits × q packets, by using r-number of packets corresponding to the least common multiple of M ÷ s =p and N ÷ s=q as one unit (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36; as shown in Figure 2 the 2nd FIFO contains a plurality (4) of data [containing 8 packets] in a 16-bit format that are converted into a plurality of data (2) [containing the same 8 packets] in a 32-bit format and stored in a 1st FIFO).

For claims 12, 30, 38 and 40:

A data transmission method, which processes data through an N-bit bus, comprising a multi-format conversion step of:

- dividing N-bit (32) format data into packets of s-bits (8) that correspond to the greatest common measure of N (32) and M (16) (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36); and
- converting p-number (2) of data having an N-bit format constituted by s bits (8) × q (4) packets to q-number of data having an M-bit format constituted by s bits × p packets, by using r-number of packets corresponding to the least common multiple of M ÷ s=p and N ÷ s=q as one unit (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36; as shown in Figure 2 the 1st FIFO contains a plurality (2) of data [containing 8 packets] in a 16-bit format that are converted into a plurality of data (4) [containing the same 8 packets] in a 32-bit format and stored in a 2nd FIFO).

8. Claims 13-18 and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon as applied to claims 1-4, 11-12, 19-22, and 29-30 above, and further in view of Sound On Sound "More Bits For Your Bucks".

Kwon teaches a data transmission method and apparatus for bi-directional transfer of data between two buses with different widths. In particular Kwon teaches converting M-bit format data to N-bit format data (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36); and

transmitting the converted N-bit format data to a data processing device (Fig. 2; col. 3, ll. 19-25; col. 3, line 58 – col. 4, line 36). Kwon further teaches that M-bit (16) data is converted to N-bit (32) data through the use of common size byte packets that are transferred between buffer memories. Kwon continues to teach, "One of ordinary skill in the art can use the teachings of the present invention to other devices requiring bi-directional transfer of data between buses with different data word width."

Sound On Sound (hereinafter SOS) teach of the Terratec EWS88MT PCI Soundcard for the PC. The EWS88MT supports 24-bit, 96kHz digital audio signals for superior sound quality. With such a high quality data format there is a huge increase in the amount of data being shunted to and fro. In order to fully maximize transactions on the 32-bit PCI bus (to which the sound card connects) four 24-bit words may be 24-bit packed into a stream of 32-bit PCI transactions (page 2). "All transfers across the PCI buss are 32 bits wide, so 24-bit packed transfers send 24 bits of the first sample and the first 8 bits of the second, followed by the final 16 bits of the second and the first 16 bits of the third, the final 8 bits of the third followed by the entire 24 bits of the fourth, and so on (page 2)."

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the 24-bit audio data of SOS as M-bit data of Kwon such that the audio data can be easily converted into 32-bit bus compliant data using four 8-bit packets that maximize transfers across the 32-bit bus.

Allowable Subject Matter

9. Claims 5-10 and 23-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. *Please see the Office Action dated October 31, 2005 for the Examiner's reasons for indicating allowable subject matter.*

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

RMS

PAUL R. MYERS
PRIMARY EXAMINER